09/807500

Class	Subclass

ISSUE CLASSIFICATION

PATENT NUMBER

U.S. **UTILITY** Patent Application

O.I.P.E.	PATENT DATE
SCANNED H Hkm 3a.a. 2113	

APPLICATION NO.	CONT/PRIOR	CLASS	SUBCLASS	ART UNIT	EXAMINER
09/807500	D	[redacted]	=	[redacted] 2709	DO

APPLICANTS

Rakesh Malik
Puneet Goel

708 300 2124

TITLE

Area efficient realization of coefficient architecture for bit-serial fir, iir filters and combinational/sequential logic structure with zero latency clock output

PTO-2040
12/99

ISSUING CLASSIFICATION

ORIGINAL		CROSS REFERENCE(S)	
CLASS	SUBCLASS	CLASS	SUBCLASS (ONE SUBCLASS PER BLOCK)
INTERNATIONAL CLASSIFICATION			
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☐ TERMINAL DISCLAIMER	DRAWINGS			CLAIMS ALLOWED	
	Sheets Drwg.	Figs. Drwg.	Print Fig.	Total Claims	Print Claim for O.G.
☐ The term of this patent subsequent to _____ (date) has been disclaimed.	_____ (Assistant Examiner) _____ (Date)			NOTICE OF ALLOWANCE MAILED	
☐ The term of this patent shall not extend beyond the expiration date of U.S Patent. No. _____	_____ (Primary Examiner) _____ (Date)			ISSUE FEE	
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